FORM PTO-1449

INFORMATION DISCLOSURE STATEMENT

ATTY. DOCKET NO. 1875.2800001	APPLICATION NO. 10 720/44
APPLICANT Mulder et al. , /	
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tel	ÄR	1	Abo, A.M. and Gray, P.R., "A 1.5-V, 10-bit, 14.3-MS/s CMOS Pipeline Analog-to-Digital Converter," IEEE Journal of Solid-State Circuits, IEEE, Vol. 34, No. 5, May 1999, pp. 599-606.							
All	AS	<u>1</u>	9.5 Effect	Brandt, B.P. and Lutsky, J., "A 75-mW, 10-b, 20-MSPS CMOS Subranging ADC with 9.5 Effective Bits at Nyquist," <i>IEEE Journal of Solid-State Circuits</i> , IEEE, Vol. 34, No. 12, December 1999, pp. 1788-1795.						
AU	AT	1	Bult, Klaa mm³," <i>IEEE</i> pp. 1887-1	E Journal of So	d, Aaron, "An Embedded : Solid-State Circuits, IE	240-mW 10-b 5	0-MS/s 'CMC No. 12, D	OS ADC in 1- ecember 1997,		
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FORM PTO-1449

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pu	Cho, T.B. and Gray, P.R., "A 10 b, 20 Msample/s, 35 mW Pipeline A/D Converter,"  IEEE Journal of Solid-State Circuits, IEEE, Vol. 30, No. 3, March 1995, pp. 166-  172.									
ALL	AS	2	Dackground	Choe, M-J. et al., "A 13-b 40-Msamples/s CMOS Pipelined Folding ADC with Background Offset Trimming," <i>IEBE Journal of Solid-State Circuits</i> , IEBE, Vol. 35, No. 12, December 2000, pp. 1781-1790.						
th	AT 2	<u>2</u>	Choi, M. ar Journal of 1858.	nd Abidi, A., Solid-State C	"A 6-b l.3-Gsample/s A/D Circuits, IBBE, Vol. 36, N	Converter i	n 0.35-μm mber 2001	CMOS," <i>IEEE</i>		
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Page 3 of 11

FORM PTO-1449

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HU	Flynn, M. and Sheahan, B., "A 400-Msample/s, 6-b CMOS Folding and Interpolating									
KW	AS	<u>3</u>	Geelen, G. State Circ	Geelen, G., "A 6b 1.1GSample/s CMOS A/D Converter," IEEE International Solid- State Circuits Conference, IEEE, 2001, pp. 128-129 and 438.						
the state of the s	AT	<u>3</u>	in 0.8 mm <sup>3</sup>	G. and Roover ," <i>IEEE Journ</i> 1999, pp. 1796	rs, R., "A 65-mW, 10-bit, 40- nal of Solid-State Circuits, 5-1802.	-Msample/	s BiCMOS I 1. 34, No	Nyquist ADC		
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M	AS	Ingino, J.M. and Wooley, B.A., "A Continuously Calibrated 12-b, 10-MS/s, 3.3-V A/D Converter," IEEE Journal of Solid-State Circuits, IEEE, Vol. 33, No. 12, December 1998, pp. 1920-1931.							
AU	AT	Ito, M. e Solid-Sta	Ito, M. et al., "A 10 bit 20 MS/8 3 V Supply CMOS A/D Converter," IEEE Journal of Solid-State Circuits, IEEE, Vol. 29, No. 12, December 1994, pp. 1531-1536.						
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MU	AS	<u>5</u>	Kusumoto, K. et al., "A 10-b 20-MHz 30-mW Pipelined Interpolating CMOS ADC," IEEE Journal of Solid-State Circuits, IEEE, Vol. 28, No. 12, December 1993, pp. 1200-1206.								
KU	AT	<u>5</u>	Lewis, S. of Solid-	Lewis, S. et al., "A 10-b 20-Msample/s Analog-to-Digital Converter," <i>IEEE Journal of Solid-State Circuits</i> , IEEE, Vol. 27, No. 3, March 1992, pp. 351-358.							
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M	OTHER (Including Author, Title, Date, Pertinent Pages, etc.)  Mehr, I. and Singer, L., "A 55-mW, 10-bit, 40-Msample/s Nyquist-Rate CMOS ADC,"  IEEE Journal of Solid-State Circuits, IEEE, Vol. 35, No. 3, March 2000, pp. 318-325.							CMOS ADC,"		
AU	AS	<u>6</u>	End," IEE	Nagaraj, K. et al., "Efficient 6-Bit A/D Converter Using a 1-Bit Folding Front End," IEEE Journal of Solid-State Circuits, IEEE, Vol. 34, No. 8, August 1999, pp. 1056-1062.						
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FORM PTO-1449

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Page 8 of 11

FORM PTO-1449

INFORMATION DISCLOSURE STATEMENT

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pa	AS	<u>8</u>		Taft, R.C. and Tursi, M.R., "A 100-MS/s 8-b CMOS Subranging ADC with Sustained Parametric Performance from 3.8 V Down to 2.2 V," IEEE Journal of Solid-State Circuits, IEEE, Vol. 36, No. 3, March 2001, pp. 331-338.							
jw.	АТ	<u>8</u>		loeg, H. and : 40S," <i>IEEE Jo</i> 1999, <b>pp</b> . 180	Remmers, R., "A 3.3-V, urnal of Solid-State ( 3-1811.	10-b 2: Circuits	5-Msample, IEEE, V	/s Two-S	tep ADC in No. 12,		
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<b>KU</b>	AS	Vorenkamp, P. and Roovers, R., "A 12-b, 60-Msample/s Cascaded Folding and Interpolating ADC," IEEE Journal of Solid-State Circuits, IEEE, Vol. 32, No. 12, December 1997, pp. 1876-1886.							
#W	AT	<u>9</u>	Wang, Y-T. Solid-Stat	and Razavi, 1 e Circuits, II	B., "An 8-bit 15 EEE, Vol. 35, No	0-MHz CMOS ;	A/D Conver	rter," <i>IEEE</i> 308-317.	Journal of
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FORM PTO-1449

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pu	AS	Yu, P.C. and Lee, H-S., "A 2.5-V, 12-b, 5-Msample/s Pipelined CMOS ADC," IEEE Journal of Solid-State Circuits, IEEE, Vol. 31, No. 12, December 1996, pp. 1854-1861.							
ra	АТ	Miyazaki et al., "A 16mW 30MSample/s 10b Pipelined A/D Converter using a Pseudo- Differential Architecture", ISSCC 2002/Session 10/High-Speed ADCs/10.5, February 5, 2002, 3 pgs.							
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